REMARKS

Applicant is in receipt of the Office Action mailed March 10, 2004.

Rejections Under Section 103

Claim 1 was rejected under 35 U.S.C. 103(a) as being unpatentable over Olszewski et al., U. S. Patent 6,339,818, Bowles, U. S. Patent 5,796,980, and in further view of Jeddeloh, U. S. Patent Application Publication 2003/0070044.

Claims 2-4 were rejected under 35 U.S.C. 103(a) as being unpatentable over Olszewski et al., U. S. Patent 6,339,818, Bowles, U. S. Patent 5,796,980, Jeddeloh, U. S. Patent Application Publication 2003/0070044, as applied to claim 1 above, and in further view of Longhenry et al., U. S. Patent 5,991,865.

Claim 5 was rejected under 35 U.S.C. 103(a) as being unpatentable over Olszewski et al., U. S. Patent 6,339,818, Bowles, U. S. Patent 5,796,980, Jeddeloh, U. S. Patent Application Publication 2003/0070044, Longhenry et al., U. S. Patent 5,991,865, as applied to claims 1, 4 above, and in further view of Crump et al., U. S. Patent 5,860,086 and Buckelew et al., U. S. Patent 6,667,774.

Claims 6, 8, and 9 were rejected under 35 U.S.C. 103(a) as being unpatentable over Olszewski et al., U. S. Patent 6,339,818, Bowles, U. S. Patent 5,796,980, Jeddeloh, U. S. Patent Application Publication 2003/0070044, as applied to claim 1 above, and in further view of Buckelew et al., U. S. Patent 6,667,774.

Claim 7 was rejected under 35 U.S.C. 103(a) as being unpatentable over Olszewski et al., U. S. Patent 6,339,818, Bowles, U. S. Patent 5,796,980, Jeddeloh, U. S. Patent Application Publication 2003/0070044, and Buckelew et al., U. S. Patent 6,667,774 as applied to claims 1, 6 above, and in further view of Crump et al., U. S. Patent 5,860,086.

Claim 10 was rejected under 35 U.S.C. 103(a) as being unpatentable over Olszewski et al., U. S. Patent 6,339,818, Bowles, U. S. Patent 5,796,980, Jeddeloh, U. S.

Patent Application Publication 2003/0070044, as applied to claim 1 above, and in further view of Crump et al., U. S. Patent 5,860 and Longhenry et al., U. S. Patent 5,991,865.

Claim 1 as amended recites:

> A graphics system comprising:
> one or more memories configured to receive and store graphics data, wherein each memory comprises on a single integrated chip,
> one or more RAM memories configured to store the graphics data,
> a level two cache memory connected to each RAM memory, and
> a level one cache memory connected to each of the level two cache memories;
> an array of registers configured to store status information, wherein the status information tracks and indicates accesses to the graphics data in the level one cache, wherein the status information further indicates whether the graphics data is modified or unmodified; and
> a memory request processor connected to the memories and to the array of registers, wherein the memory request processor is operable to transfer graphics data from one of the level one cache memories to one of the corresponding level two cache memories according to the status information.

Olszewski et al., U. S. Patent 6,339,818, hereafter referred to as Olszewski, neither teaches nor suggests "one or more memories configured to receive and store graphics data, wherein each memory comprises on a single integrated chip, one or more RAM memories configured to store the graphics data, a level two cache memory connected to each RAM memory, and a level one cache memory connected to each of the level two cache memories".

Instead, Olszewski teaches system level one caches and level two caches on different chips connected by buses 220 and 222 as illustrated in Figure 2B and column 4, lines 38-63:

> "With reference now to FIG. 2B, a block diagram depicts selected internal functional units of a data processing system that may include the present invention. System 200 comprises hierarchical memory 210 and processor 230. Hierarchical memory 210 typically comprises one or more Level 1 caches such as Instruction Cache 231, Data cache 235, Level 2 cache 202, random access memory (RAM) 204, and disk 206. The Level 1 caches 231 and 235 typically provide the fastest access to data and instructions that may be stored in the L2 cache 202 or RAM 204 in a manner which is well-known in the art. Although only two levels of cache are described, any number Levels of cache may be implemented in a manner which is well-known in the art. RAM 204 provides main memory storage for data and instructions that may also provide a cache for

data and instructions stored on nonvolatile disk 206.

> Data and instructions may be transferred to processor 230 from hierarchical memory 210 on instruction transfer path 220 and data transfer path 222. Instruction transfer path 220 and data transfer path 222 may be implemented as a single bus or as separate buses between processor 230 and hierarchical memory 210. Alternatively, a single bus may transfer data and instructions between processor 230 and hierarchical memory 210 while processor 230 provides separate instruction and data transfer paths within processor 230, such as instruction bus 232 and data bus 234."

In addition, as stated by the examiner, Olszewski does not disclose "a memory request processor connected to the memory wherein the memory request processor controls", "further indicates whether the graphics data is modified or unmodified", or the "transfer of data from the level one cache memory to the level two cache memory according to the status information".

Bowles, U. S. Patent 5,796,980, hereafter referred to as Bowles, neither teaches nor suggests "one or more memories configured to receive and store graphics data, wherein each memory comprises on a single integrated chip, one or more RAM memories configured to store the graphics data, a level two cache memory connected to each RAM memory, and a level one cache memory connected to each of the level two cache memories". Instead, Bowles teaches level one caches 20 and 25 and a level two cache 30 connected by a shared memory bus 40 to a main memory 50 as illustrated in Figure 1.

Jeddeloh, U. S. Patent Application Publication 2003/0070044, hereafter referred to as Jeddeloh, neither teaches nor suggests "one or more memories configured to receive and store graphics data, wherein each memory comprises on a single integrated chip, one or more RAM memories configured to store the graphics data, a level two cache memory connected to each RAM memory, and a level one cache memory connected to each of the level two cache memories". Instead, Jeddeloh teaches a system comprising a level 1 cache 22 embedded on a processor 20, a bus 30 connecting a separate level 2 cache 24

and a system controller 60 with an embedded level 3 cache, and a bus 34 connecting the system controller 60 and a system memory 50, as illustrated in Figure 1.

In addition, Jeddeloh, neither teaches nor suggests a system controller configured to "transfer graphics data from one of the level one cache memories to one of the corresponding level two cache memories according to the status information".

Instead, Jeddeloh teaches a system controller configured to reduce memory latency as disclosed in the summary on page 2, paragraph [0015]:

> "An integrated circuit system controller for use in a processor-based system includes a system memory controller and a level 3 cache memory embedded in the system controller. The level 3 cache memory includes a DRAM array, a tag array, and a cache memory controller coupled to the DRAM array and the tag array. The cache memory controller receives a request for access to the cache memory, and, in response thereto, preferably initiates an access to both the tag memory and the DRAM array. The cache memory controller determines on basis of the tag whether the access to the cache memory will result in a cache hit or a cache miss. If the access will result in a cache hit, the cache memory controller couples data from the DRAM array to the processor. According to one aspect of the invention, the cache memory controller initiates the access to the DRAM array before the cache memory controller determines whether the access to the cache memory will result in a cache hit or a cache miss. According to another aspect of the invention, an access to the system memory is initiated responsive to the request for access to the cache memory. The access to the system memory is preferably initiated before the cache memory controller determines whether the access to the cache memory will result in a cache hit or a cache miss. If the access will result in a cache miss, the data from the system memory is coupled to the processor."

Therefore, amended claim 1 is patentably distinguished over Jeddeloh, Bowles, and Olszewski for at least the reasons stated above. The rejections of claims 2-10 are moot in light of the amended claim 1. Claims 33 and 40 recite features similar to those recited in claim 1, and thus, claims 33 and its dependents and claim 40 are patentably distinguished over Jeddeloh, Bowles, and Olszewski based on reasoning similar to that given above in support of claim 1.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5181-86900/JCH.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

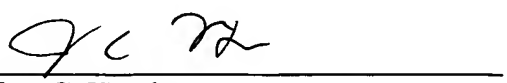
☐ Request for Approval of Drawing Changes

☒ Notice of Change of Address

☐ Check in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,



Jeffrey C. Hood
Reg. No. 35,198
ATTORNEY FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert & Goetzel PC
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800
Date: 6/10/2004